a host processor;

a storage device; and

a queue management process to configure said one or more queues on said storage device in accordance with said at least one queue parameter.

32. The circuitry of claim 31 wherein said queue management process includes a read pointer process for each queue configured by said queue management process, wherein said read pointer process is configured to specify a next read address indicative of the memory location within said storage device from which the next queue object requested from said queue is to be read.

33. The circuitry of claim 31 wherein said queue management process includes a write pointer process for each queue configured by said queue management process, wherein said write pointer process is configured to specify a next write address indicative of the memory location within said storage device to which the next queue object provided to said queue is to be written.

Cl 2 Cont'd.

34. The circuitry of claim 31 further comprising at least one slave processor.

35. The circuitry of claim 34 further comprising a data bus for connecting said host and slave processors, wherein said data bus transfers queue objects between said processors.

36. The circuitry of claim 34 further comprising a flag bus for connecting said host and slave processors.

37. The circuitry of claim 36 wherein said queue management process includes a queue status monitoring process for each queue configured by said queue management process, wherein said queue status monitoring process provides a queue status flag, which is indicative of an operational condition of said queue, on said flag bus.

38. The circuitry of claim 31 wherein said queue management process includes a queue base address process for each queue configured by said queue management process, wherein said queue base address process specifies a starting address for said queue.

39. The circuitry of claim 31 wherein said at least one queue parameter includes a queue depth parameter and said queue management process includes a queue depth specification process for each queue configured by said queue management process, wherein said queue depth specification process configures said queue in accordance with said queue depth parameter.

40. The circuitry of claim 31 wherein said at least one queue parameter includes a queue entry size parameter and said queue management process includes a queue entry size specification process for each queue configured by said queue management process, wherein said queue entry size specification process configures said queue in accordance with said queue entry size parameter.

In the drawings:

Please substitute the enclosed drawing (i.e., substitute figure 2) for the drawing (i.e., original figure 2) originally submitted with the application. Substitute figure 2 was modified to correct the text within text block 110. Namely, the label "write pointer process" was modified to " queue status monitoring process". The text block that was modified is circled in red ink on substitute drawing 2. No new matter is added.